REMARKS

Reconsideration of this application is respectfully requested. Claims 1-3, 9, 10, and 12 stand rejected under § 35 U.S.C. 102(e) as being anticipated by United States Patent number 6,023,720 by Aref et al. ("Aref"). Claims 1-17 stand rejected under 35 § U.S.C. 102(a) as being anticipated by the article titled Memory Access Scheduling by Rixner ("Rixner").

No claims have been amended. New claims 18-20 have been added.

The Examiner rejected claims 1-3, 9, 10, and 12 under 35 U.S.C. § 102(e) as being anticipated by Aref.

However, applicant respectfully asserts that claim 1 is not anticipated by Aref under 35 U.S.C. § 102(e). Claim 1 states:

> 1. A process for scheduling requests to access a resource, said requests originating from at least one thread from at least one initiator, said process comprising combining scheduling of requests between threads and scheduling of requests of initiator access to the resource and maintaining order of requests within each thread.

(emphasis added)

Aref discloses a disk scheduling system that makes no attempt to maintain the issue order of read or write requests within a stream. The order of read or write requests is allowed to be re-ordered to satisfy disk scheduling efficiency requirements. An additional mechanism called a Sequence Control Broker outside of the disk scheduling mechanism is forced take care of re-ordering the stream as needed to re-establish the original issue order. Aref discloses:

> Seek time is the most time-consuming part of disk retrieval. One purpose of disk scheduling algorithms is to reduce this seek time. This can be achieved by queuing and ordering the disk access requests so that seek time is minimized.

(Col. 4 Lns. 29-34) (emphasis added)

Aref further discloses:

> In order to retrieve the video in the correct order, a Sequence Control Broker (SCB) 14 stores an ordered list of pointers to all the MSF blocks of a video stream. The SCB 14 acts on behalf of users to maintain a video playback stream.

(Col. 3 Lns. 45-48) (emphasis added)

Aref does not disclose or suggest a process to schedule requests to access a resource and maintain order of requests within each thread. In contrast, Aref suggests a disk scheduling system to minimize seek time at the expense of having to reorder disk access requests. Therefore, Aref does not disclose each and every limitation of claim 1. As such, claim 1 is not anticipated by Aref under 35 U.S.C. § 102(e).

Given that claims 2, 3, and 9 depend from and include the limitations of claim 1, claims 2, 3, and 9 are also not anticipated by Aref under 35 U.S.C. § 102(e).

Applicant respectfully asserts that independent claim 10 is not anticipated by Aref under 35 U.S.C. § 102(e). Claim 10 states:

> 10. A scheduling apparatus for scheduling access to a resource, comprising:
> an input coupled to receive at least one access request originating from at least one thread from at least one initiator;
> logic to combine scheduling of requests between threads and scheduling of initiator access to the resource and maintaining order of requests within each thread.

(emphasis added)

As discussed above, Aref does not disclose or suggest a scheduling apparatus having logic to maintain the order of requests within each thread. In contrast, Aref discloses and suggests a disk scheduling system to minimize seek time at the expense of having to reorder disk access requests with a Sequence Control Broker. Therefore, Aref does not disclose each and every limitation of claim 10. As such, claim 10 is not anticipated by Aref under 35 U.S.C. § 102(e).

Given that claim 12 depends from and includes the limitations of claim 10, claim 12 is also not anticipated by Aref under 35 U.S.C. § 102(e).

Applicant respectfully asserts that independent claim 18 is not anticipated by Aref under 35 U.S.C. § 102(e). Claim 18 states:

> 18. An apparatus, comprising:
> means for scheduling requests to access a resource, wherein the requests originate from at least one thread of at least one initiator;
> means for combining scheduling of requests between threads; and
> means for scheduling of requests of initiator access to the resource and maintaining order of requests within each thread.

(emphasis added)

As discussed above, Aref does not disclose or suggest a means for maintaining the order of requests within each thread. In contrast, Aref discloses and suggests a disk scheduling system to minimize seek time at the expense of having to reorder disk access requests with a Sequence Control Broker. Therefore, Aref does not disclose each and every limitation of claim 18. As such, claim 18 is not anticipated by Aref under 35 U.S.C. § 102(e).

Claims 1-17 stand rejected under 35 § U.S.C. 102(a) as being anticipated by Rixner.

However, applicant respectfully asserts that claim 1 is not anticipated by Rixner under 35 U.S.C. § 102(a). Claim 1 states:

> 1. A process for scheduling requests to access a resource, said requests originating from at least one thread from at least one initiator, said process comprising combining scheduling of requests between threads and scheduling of requests of initiator access to the resource and maintaining order of requests within each thread.

(emphasis added)

Rixner discloses a memory access scheduling scheme that completes memory requests out of order and uses reorder buffers to fix up any memory ordering problems encountered.

Rixner discloses:

> This paper introduces memory access scheduling in which DRAM operations are scheduled possibly completing memory references out of order, to optimize memory system performance.

(Page 1, Third Paragraph) (emphasis added)

> Section 3 introduces the concept of memory access scheduling and the possible algorithms that can be used to reorder DRAM operations.

(Page 2 Second Paragraph) (emphasis added)

> The imagine streaming memory system consists of a pair of address generators, four interleaved memory bank controllers and a pair of reorder buffers that place stream data in the SRF in the correct order.

(Page 5 Last Paragraph) (emphasis added)

> The aggressive scheduling algorithms improve the memory bandwidth of the microbenchmarks by . . .85-93% over in-order scheduling.

((Page 8 Fourth Paragraph) (emphasis added)

Rixner does not disclose or suggest a process to schedule requests to access a resource and maintain order of requests within each thread. In contrast, Aref suggests a DRAM scheduling system to optimize performance at the expense of having to reorder disk access requests. Therefore, Rixner does not disclose each and every limitation of claim 1. As such, claim 1 is not anticipated by Rixner under 35 U.S.C. § 102(a).

Given that claims 2-9 depend from and include the limitations of claim 1, claims 2-9 are also not anticipated by Rixner under 35 U.S.C. § 102(a).

Applicant respectfully asserts that independent claim 10 is not anticipated by Rixner under 35 U.S.C. § 102(a). Claim 10 states:

> 10. A scheduling apparatus for scheduling access to a resource, comprising:
> an input coupled to receive at least one access request originating from at least one thread from at least one initiator;
> logic to combine scheduling of requests between threads and scheduling of initiator access to the resource and maintaining order of requests within each thread.

(emphasis added)

As discussed above, Rixner does not disclose or suggest a scheduling apparatus having logic to maintain the order of requests within each thread. In contrast, Rixner discloses and suggests a memory access scheduling system to optimize performance at the expense of having to reorder disk access requests with a Sequence Control Broker. Therefore, Rixner does not disclose each and every limitation of claim 10. As such, claim 10 is not anticipated by Rixner under 35 U.S.C. § 102(a).

Given that claims 11-17 depend from and include the limitations of claim 10, claims 11-17 are also not anticipated by Rixner under 35 U.S.C. § 102(a).

Applicant respectfully asserts that independent claim 18 is not anticipated by Rixner under 35 U.S.C. § 102(a). Claim 18 states:

> 18. An apparatus, comprising:
> means for scheduling requests to access a resource, wherein the requests originate from at least one thread of at least one initiator;
> means for combining scheduling of requests between threads; and
> means for scheduling of requests of initiator access to the resource and maintaining order of requests within each thread.

(emphasis added)

As discussed above, Rixner does not disclose or suggest a means for maintaining the order of requests within each thread. In contrast, Rixner discloses and suggests an aggressive algorithm for memory access scheduling system to optimize performance at the expense of having to reorder disk access. Therefore, Rixner does not disclose each and every limitation of claim 18. As such, claim 18 is not anticipated by Rixner under 35 U.S.C. § 102(a).

Given that claims 19 and 20 depend from and include the limitations of claim 18, claims 19 and 20 are also not anticipated by Rixner under 35 U.S.C. § 102(a).

CONCLUSION

It is respectfully submitted that in view of the amendments and remarks set forth herein, the rejections and objections have been overcome. Applicant requests the issuance of a timely notice of allowance. Applicant reserves all rights with respect to the application of the doctrine equivalents. If there are any additional charges, please charge them to our Deposit Account No. 02-2666.

Respectfully submitted,
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